

## **Comparative analysis of various asymmetrical configurations of cascaded H-Bridge multilevel converter**

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**Abstract:** *The main objective of asymmetrical multilevel converter configuration is to achieve quality form of AC voltage and current by increasing the levels of output voltage. This paper mainly investigate the pro's and con's of various dc source progression schemes like binary, quasi, trinary, etc proposed for the asymmetrical cascaded H bridge multilevel converter topologies. The performance of a 3 $\phi$ , 400V cascaded Three H Bridge multilevel converter has been examined for various asymmetrical dc source progression schemes using MATLAB/Simulink and also prototype converter has been validated using dSPACE DS1103 real time interface controller.*

**Key words** - *Asymmetrical dc source progression, cascaded H-Bridge multilevel converter, %THD, multicarrier PWM*

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### **I. Introduction**

In recent years the multilevel converters (MLC) are really suitable alternate for conventional two level converters in industries. The objective of MLC is not only converting dc into ac but also providing quality form of output with less harmonic contents than the two level converters. The concept of MLC is the sum of the voltages by the commutation of switches to produce the staircase sinusoidal shaped ac output voltage. The MLC has emerged the solution for medium and high power applications. Low EMI, less dv/dt on switches, low switching losses recommends MLC to be used in transmission system, industrial drives, power conversion system, etc [1]-[6]. The MLC is broadly classified into three types as follows Neutral point clamped MLC, flying capacitor MLC and cascaded H Bridge MLC (CHBMLC). All the three types have unique features but comparatively CHBMLC is one step ahead than others based on its merits [16]-[17]. Unlike the other two MLC, the CHBMLC requires fewer passive components and also the operation is quite easy. The CHBMLC requires more than one dc sources which may also be replaced by photovoltaic system.

The CHBMLC further classified as symmetrical and asymmetrical configurations based on the selection of dc voltage sources. In symmetrical configuration all the dc source voltages are equal in magnitude whereas in asymmetrical configuration each dc voltage sources are unequal in magnitude [2]. However symmetrical CHBMLC has its merits such as same power rating switches, ease generation of switching pulses, and no voltage balancing issues, etc, it is not able to develop more levels in output so as to reduce THD than asymmetrical configuration for the same structure.

In asymmetrical CHBMLC Typical voltage source progressions such as unary, binary, quasi, trinary and other developed progressions are used to produce stair case output. In this paper characteristic of all the aforesaid progressions are discussed and implemented for the 3 $\phi$  ACHBMLC topology using MATLAB Simulink. The merits, demerits and the observations in THD also tabulated and discussed. The trinary progression has been implemented using dSPACE 1103 controller for validation and the observations are shown.

### **II. CHBMLC**

The conventional cascaded H Bridge MLC is formed by number of series connected H bridge units. Each H bridge unit consist of four power switches with anti-parallel diode is shown in fig 2.1 [2]. The right diagonal switches  $S_1$  and  $S_2$  are jointly used to connect source and load in positive direction and the left diagonal switches  $S_{11}$  and  $S_{22}$  are jointly used to connect source and load in negative directions. The combination of top parallel switches or bottom parallel switches is used to bypass the source from load. The top and bottom switch in each leg operates in complementary manner and at any instant two switches will be in function.

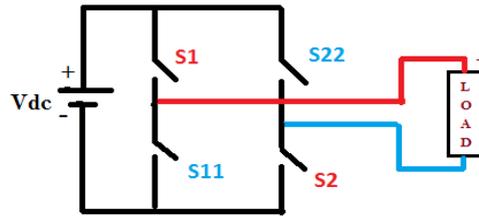


Fig 2.1 H Bridge unit

### 2.1. Asymmetrical CHBMLC

In asymmetrical MLC configuration the arrangement of dc sources is the key factor to obtain the maximum output level [9]-[13]. At present many reduced MLC topologies have been developed alternate to CHBMLC, the major drawback is that it does not operate for all dc source progression methods. Even though the conventional topology has many switches compared to reduced switch topologies, generation of output voltage levels by CHBMLC is not limited and has every possibility to use all the natural number progression schemes. The characteristics of aforementioned arrangements of DC source schemes are as follows.

If the progression of dc sources is unary, the magnitudes of voltage source ( $V_s$ ) and output voltage level ( $m$ ) obtained for  $n$  number of sources can be expressed by

$$V_n = n V_{dc}, \quad n \geq 1 \quad (2.1a)$$

$$m = 2n+1, \quad n \geq 1 \quad (2.1b)$$

For odd number progression of dc sources the given equations are

$$V_n = \begin{cases} n V_{dc}, & n = 1 \\ 2 + V_{n-1}, & n \geq 2 \end{cases} \quad (2.2a)$$

$$m = 2n^2+1, \quad n \geq 1 \quad (2.1b)$$

If the progression of dc sources is binary, then

$$V_n = 2^{(n-1)} V_{dc}, \quad n \geq 1 \quad (2.3a)$$

$$m = 2^{(n+1)}-1, \quad n \geq 1 \quad (2.3b)$$

For quasi progression, the equations are

$$V_n = \begin{cases} n V_{dc}, & n = 1 \\ 2 \times 3^{(n-2)} V_{dc}, & n \geq 2 \end{cases} \quad (2.4a)$$

$$m = \begin{cases} 3^n, & n = 1 \\ 1 + \sum_{n=2}^{\infty} 2 \times 3^{n-1}, & n \geq 2 \end{cases} \quad (2.4b)$$

For trinary progression of dc sources the equations are

$$V_n = 3^{(n-1)} V_{dc}, \quad n \geq 1 \quad (2.5a)$$

$$m = 3^n, \quad n \geq 1 \quad (2.5b)$$

From the literature, the aforesaid progressions are the popular progression schemes. Also the researchers has developed some scheme of arrangements of dc sources, the following two progressions are also used to generate the maximum levels in output voltage like above said schemes [3].

The following equations represent the Luo and Ye progressions respectively.

$$V_n = \begin{cases} n V_{dc} , & n \leq 2 \\ 7X3^{(n-3)}V_{dc}, & n \geq 3 \end{cases} \quad (2.6a)$$

$$m = \begin{cases} 3^n, & n = 1 \\ 7X3^{n-2}, & n \geq 2 \end{cases} \quad (2.6b)$$

$$V_n = \begin{cases} n^2 - u(n-2)V_{dc}, & n \leq 3 \\ 25X3^{(n-4)}V_{dc}, & n \geq 4 \end{cases} \quad (2.7a)$$

$$m = \begin{cases} 3^n, & n \leq 2 \\ 25X3^{n-3}, & n \geq 3 \end{cases} \quad (2.7b)$$

### III. Proposed System

This paper explains the characteristics of aforesaid progressions on the variations in RMS and peak values of  $V_{ph}$ ,  $V_{Line}$ ,  $I_{load}$  and % THD for the following two cases. Fig 3.1 shows the 3 $\phi$  three H Bridge systems.

Case i. The generation of 3 $\phi$ , 400V, 50 Hz with 3 H bridge per phase at the switching frequency of 2 KHz.

Case ii. For the generation of 3 $\phi$ , 400V, 50 Hz with 3 H bridge per phase at the switching frequency of 20 KHz.

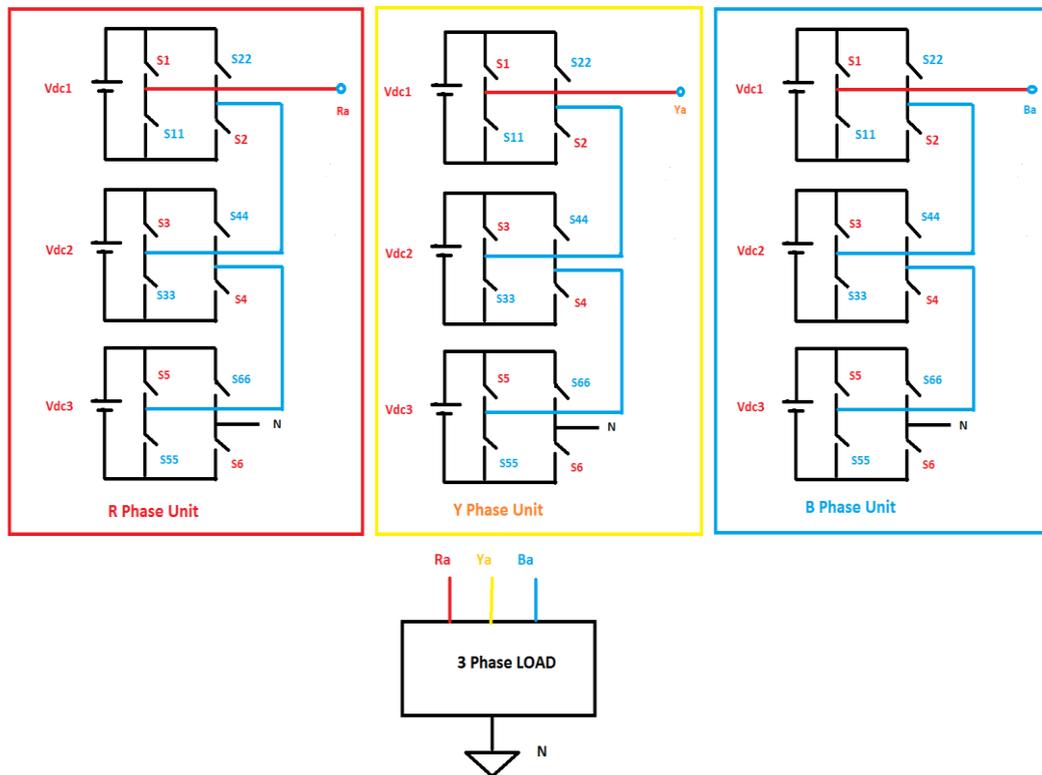


Fig 3.1 Schematic of Three phase cascaded 3H Bridge system

The three phase cascaded H Bridge system formed by series connection of 3 H Bridges per phase associated with a three phase balanced star connected load and separate dc voltage source is connected in each H bridge. The pair of switches ( $S_1, S_{11}$ ), ( $S_2, S_{22}$ ), ( $S_3, S_{33}$ ), ( $S_4, S_{44}$ ), ( $S_5, S_{55}$ ) and ( $S_6, S_{66}$ ) have been operated in complementary manner in order to avoid short circuiting. For the above system the selection of three separate input voltages  $V_{dc1}$ ,  $V_{dc2}$ ,  $V_{dc3}$  per phase for the aforementioned progression is tabulated below in table 3.1.

Table 3.1 Selection of input voltages  $V_{dc1}$ ,  $V_{dc2}$ ,  $V_{dc3}$  per phase for various schemes

Schemes/ sources	Binary (in volts)	Quasi (in volts)	Luo (in volts)	Ye (in volts)	Trinary (in volts)
$V_{dc1}$	46.5	36.15	32.5	27.1	25
$V_{dc2}$	93	72.3	65	81.3	75
$V_{dc3}$	186	216.9	227.5	216.8	225

The basic operation of the switches for the 3φ Three H Bridge system has been tabulated in look up table 3.2.

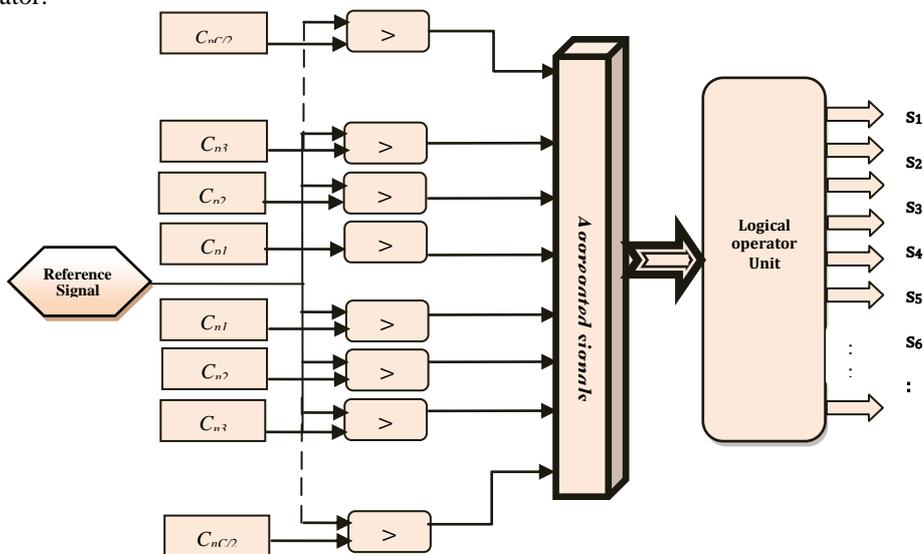
**Table 3.2 Look up table for Switching states of various output voltages**

Output voltage	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	S <sub>5</sub>	S <sub>6</sub>
$V_{dc3} + V_{dc2} + V_{dc1}$	On	On	On	On	On	On
$V_{dc3} + V_{dc2}$	On	Off	On	On	On	On
$V_{dc3} + V_{dc2} - V_{dc1}$	Off	Off	On	On	On	On
$V_{dc2} + V_{dc1}$	On	On	On	On	On	Off
$V_{dc2}$	On	Off	On	On	On	Off
$V_{dc2} - V_{dc1}$	Off	Off	On	On	On	Off
$V_{dc1}$	On	On	On	Off	On	Off
0	On	Off	On	Off	On	Off
$-(V_{dc1})$	Off	Off	On	Off	On	Off
$-(V_{dc2} - V_{dc1})$	On	On	Off	Off	On	Off
$-(V_{dc2})$	On	Off	Off	Off	On	Off
$-(V_{dc2} + V_{dc1})$	Off	Off	Off	Off	On	Off
$-(V_{dc3} + V_{dc2} - V_{dc1})$	On	On	Off	Off	Off	Off
$-(V_{dc3} + V_{dc2})$	On	Off	Off	Off	Off	Off
$-(V_{dc3} + V_{dc2} + V_{dc1})$	Off	Off	Off	Off	Off	Off

#### IV. Multicarrier PWM Switching Techniques

Multilevel converters are mostly controlled with sinusoidal PWM extended to multicarrier arrangements of two types. The multicarrier PWM schemes are broadly classified as vertically disposed and horizontally disposed carrier schemes. The vertically disposed carrier scheme further classified as Phase Disposition (PD), Phase opposite disposition (POD) and Alternate Phase opposite disposition (APOD) [15] - [19]. In all above said schemes the number of unipolar carriers ( $C = m - 1$ ) can be placed above and below zero level evenly in vertical order. The carriers positioned above and below the zero level are represented by  $C_p$  and  $C_n$  respectively. Although in horizontally disposed scheme number of bipolar carriers can be placed with uniform phase shift. Comparatively vertically disposed carrier provides better results than the above technique and also this have been more often used in practice.

The principle of PWM pulse generation is continuous comparison of the carrier signals with the reference signal. The carrier signals may be triangular wave, saw tooth wave, trapezoidal wave, semi sine wave, etc. similarly the reference signals can be sin wave, triangular wave, trapezoidal wave, etc [7]-[9]. In this work the switching frequency has been chosen as 2 KHz and 20 KHz for analysis and the frequency of reference signal has been chosen as 50Hz. Also the switching pulses have been generated with triangular carrier and sinusoidal reference signal by the possible vertically disposed schemes. The constant dc carriers with uniform increment have also been chosen as carrier signal. The fig 4.1 below shows the block diagram of switching pulse generator.



**Fig 4.1 Block diagram representation of switching pulse generator**

##### 4.1 Vertically disposed carrier techniques

In the vertically disposed carrier technique the unipolar triangular wave carriers  $C$  has been arranged evenly by the plane of above and below the zero level. These carrier waves have same frequency and same height but it has been arranged vertically in incremental order.

A sinusoidal reference signal has been compared to amplitude of each and every carrier signals produces the PWM pulses whenever the amplitude of sinusoidal signal is greater than or equals. As a result the collection of PWM signals assist to fabricate the switching pulses for each switch by logical operators.

#### 4.1.1 PD technique

In PD technique all the carriers are in-phase as the name implies and has same amplitude and frequency. Usually Phase Disposition PWM (PDPWM) has better output voltage quality with lower harmonic distortion. However, when used with cascaded multilevel converters, this method produces uneven voltage source, which disables the harmonic cancelations [1]. The PD technique is shown in fig 4.2

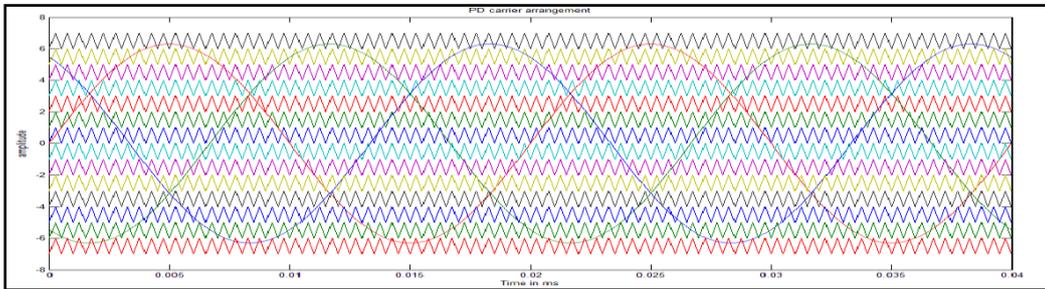


Fig 4.2 Arrangement of carrier signals in PD technique

#### 4.1.2 POD technique

In POD technique the carriers in above the zero axes have 180° phase shift to the carriers in below the zero axis but with the same amplitude and frequency. The POD technique is shown in fig 4.3

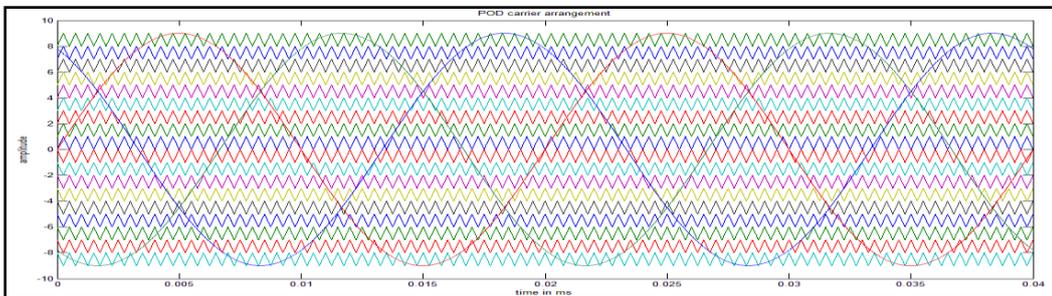


Fig 4.3 Arrangement of carrier signals in POD technique

#### 4.1.3 APOD technique

In APOD technique alternate carriers are in-phase and adjacent carriers are out of phase. The APOD technique is shown in fig 4.4

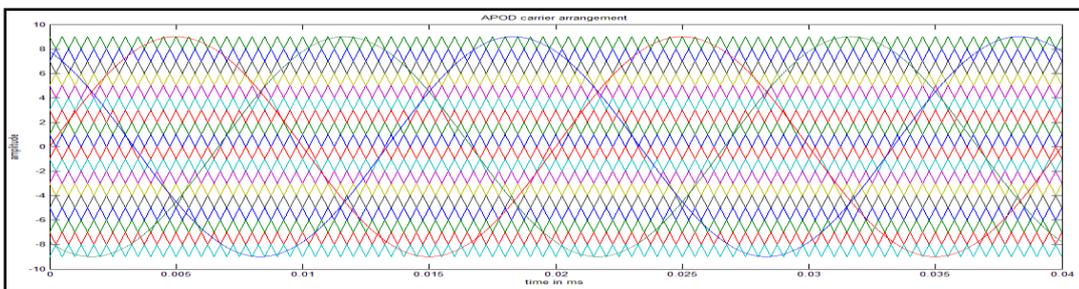


Fig 4.4 Arrangement of carrier signals in APOD technique

#### 4.1.4 Constant Carrier (CC) technique

In this technique the constant signals have been chosen as carrier signals and these carriers has different amplitude with uniform increment. Unlike the above techniques CC technique has no frequency and so no phase angle variation. In this method width of the pulses can be varied by adjusting the amplitude the signals. The base amplitude of carrier signal has been assumed to be 0.5 and 0.6 and which is approximately equals to the switching frequency of the triangular carriers  $f_s = 2$  KHz and 20 KHz respectively. Fig 4.5 shows the arrangement of CC PWM technique for a 19 level MLC.

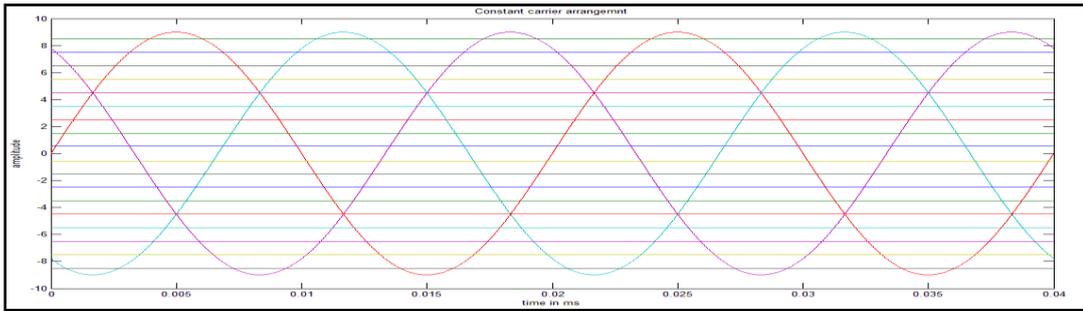


Fig 4.5 Arrangement of carrier signals in CC technique

### V. Simulation Results And Discussion

The output RMS values of phase voltage, line voltage, current and its harmonic profile in % have been compared in following order.

- 5.1. Comparisons based on switching frequency and switching techniques
- 5.2. Comparisons based on overall performance of progression for different ma

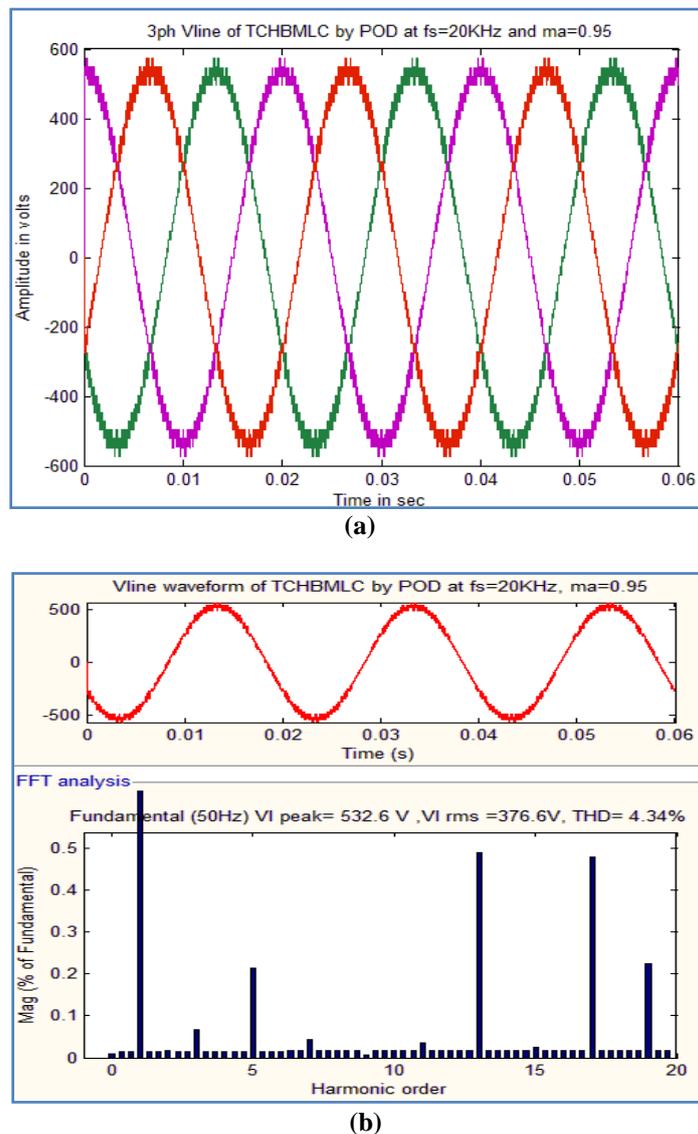
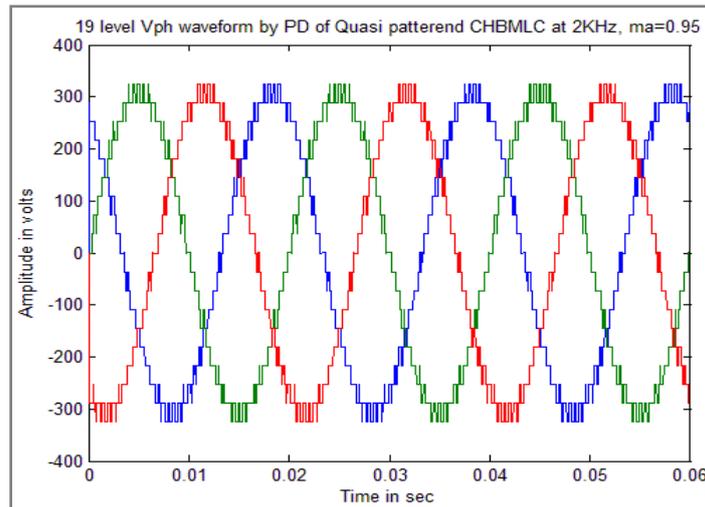
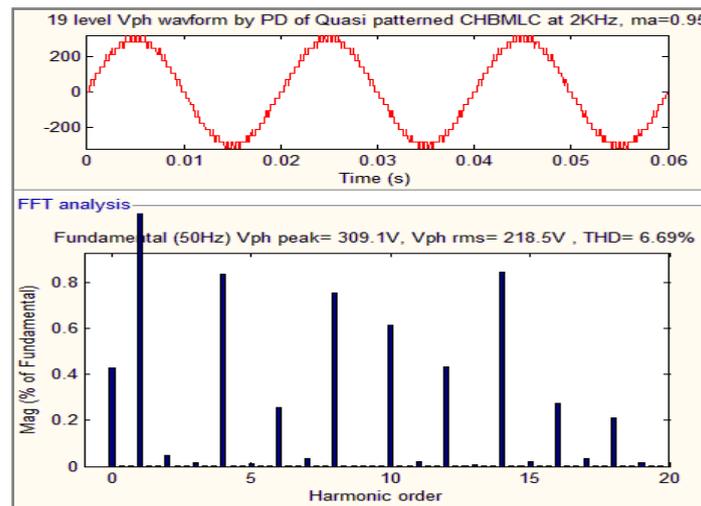


Fig 5.1 Line to line voltages of TCHBMLC by POD technique at ma=0.95 and fs=20 KHz (a)  $V_L$  Waveform (b) Harmonic profile

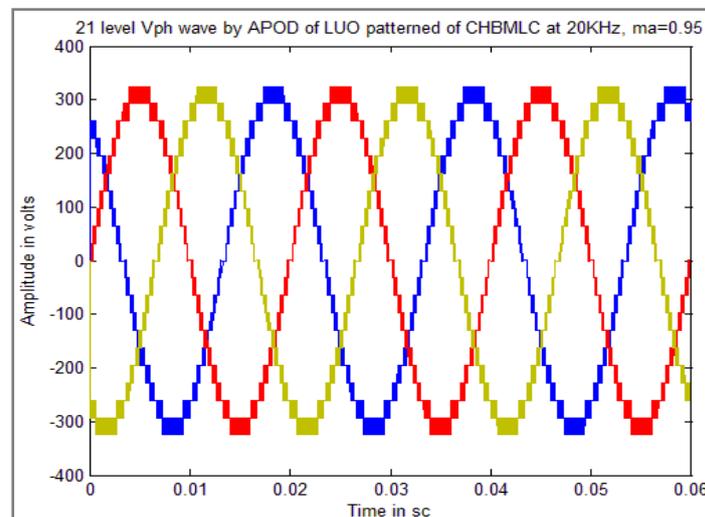


(a)

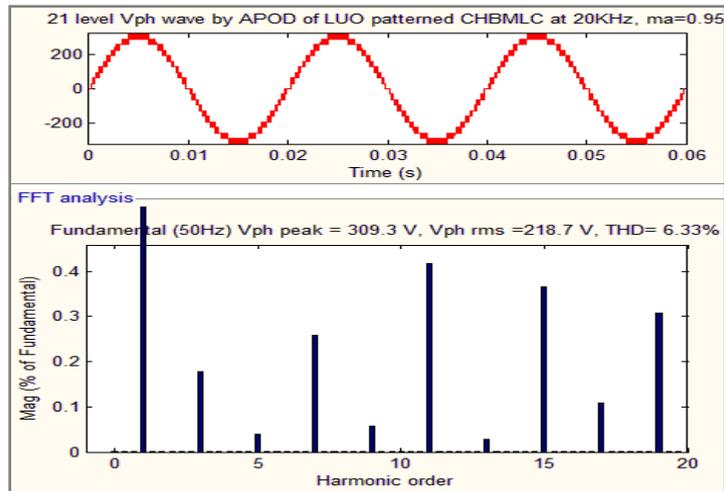


(b)

Fig 5.2 19 level three phase voltages of QCHBMLC by PD technique at ma=0.95 and fs=2 KHz (a) Vph Waveform (b) Harmonic profile

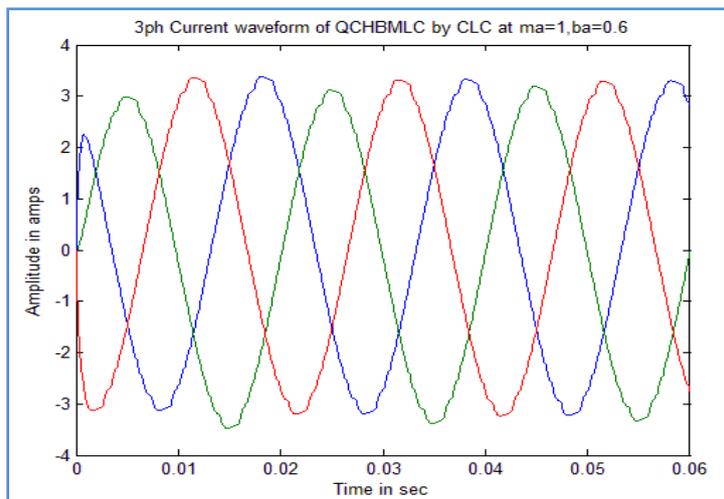


(a)

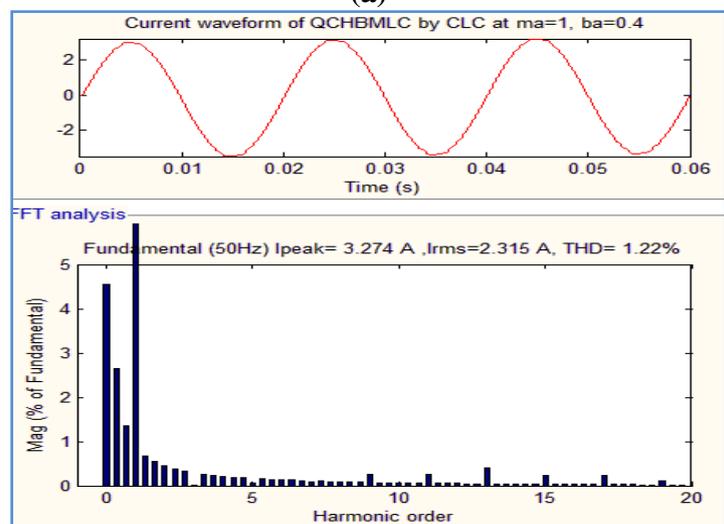


(b)

Fig 5.3 21 level three phase voltages of LCHBMLC by APOD technique at ma=0.95 and fs=20 KHz (a) Vph Waveform (b) Harmonic profile



(a)



(b)

Fig 5.4 3ph current of QCHBMLC by CLC technique at ba=0.6 and ma=1 (a) I<sub>out</sub> Waveform (b) Harmonic profile

The figs 5.1 (a), 5.2 (a), 5.3 (a) and 5.4 (a) represents the typical 3 $\phi$  line to line voltages, Phase voltage and load current waveforms obtained by Trianry, Quasi, Luo and Quasi progression schemes for 3 $\phi$ , 400V, 50 Hz system. Fig 5.1(b), 5.2(b) 5.3(b) and 5.4 (b) represents select harmonic profile of the above said output parameters. Similarly for all above said progression schemes the amplitude and harmonic content of the output parameters have been calculated and charted as follows.

**5.1 Comparisons based on switching frequency and switching techniques**

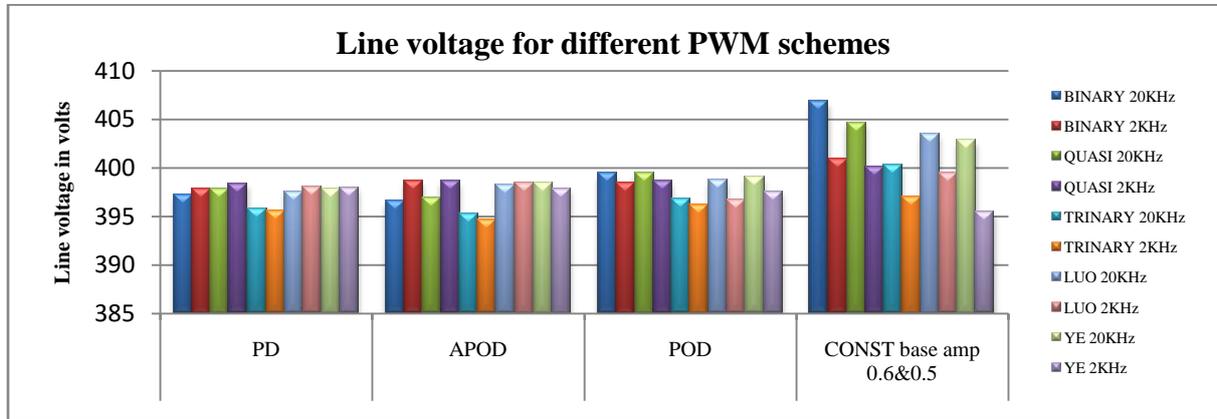


Fig 5.5 (a) RMS value of V<sub>L</sub> for different PWM schemes for m<sub>a</sub> = 1 at f<sub>s</sub>= 2 and 20 KHz

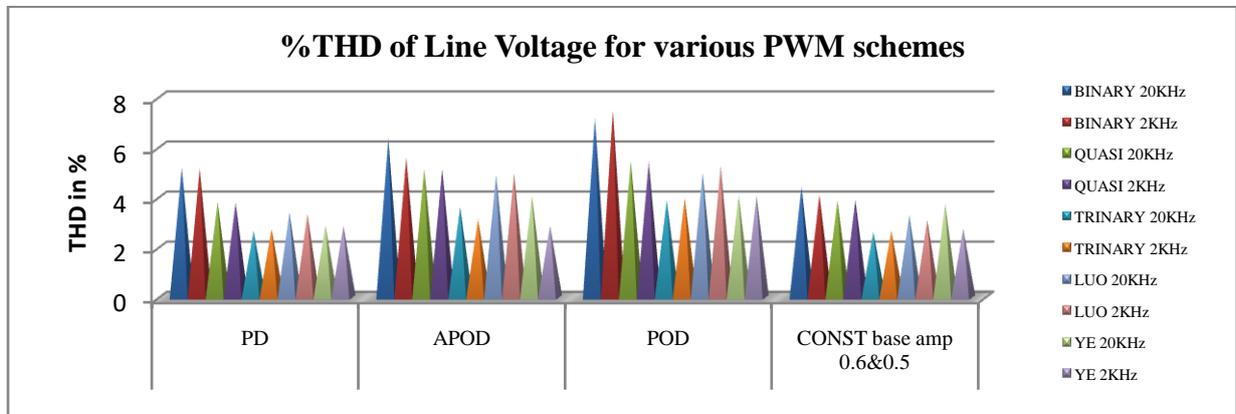


Fig 5.5 (b) %THD of V<sub>L</sub> for various PWM schemes for m<sub>a</sub> = 1 at f<sub>s</sub>= 2 and 20 KHz

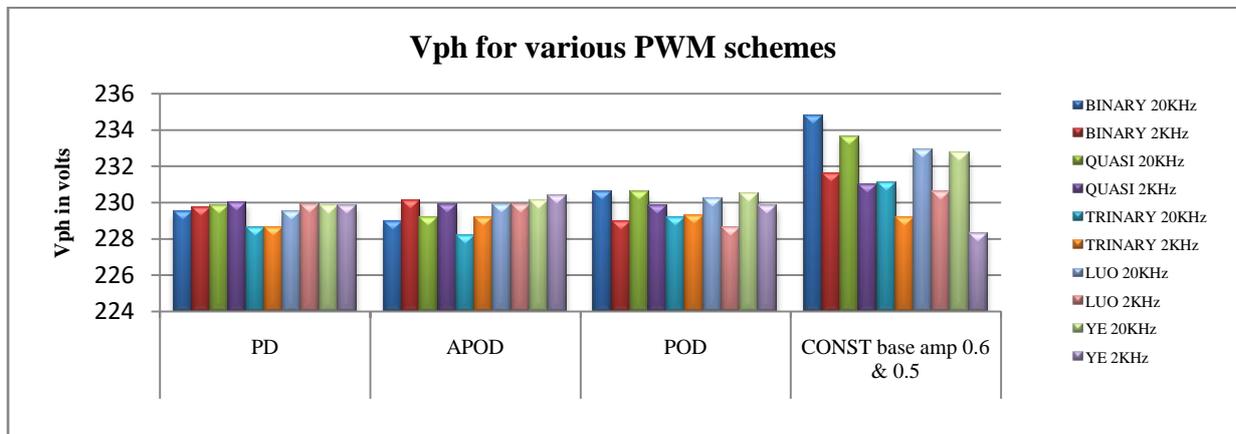


Fig 5.6 (a) RMS value of V<sub>ph</sub> for various PWM schemes for m<sub>a</sub> = 1 at f<sub>s</sub>= 2 and 20 KHz

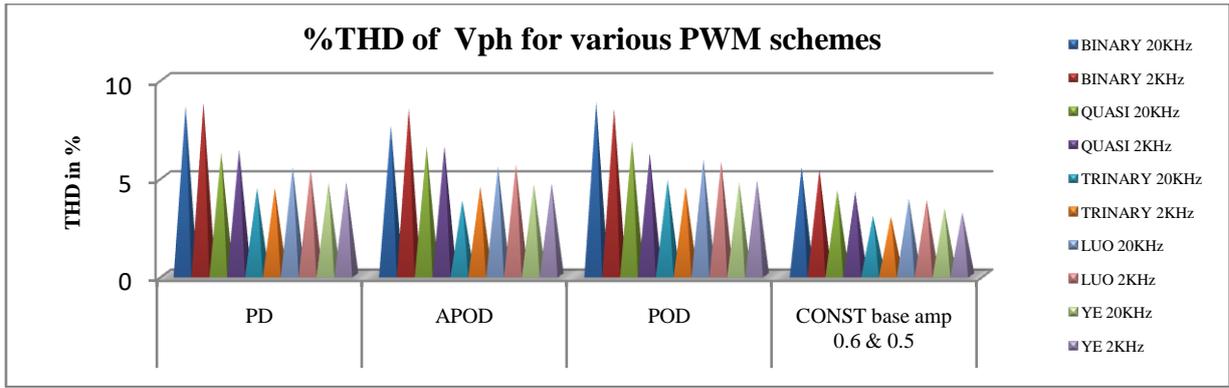


Fig 5.6 (b) %THD of Vph for various PWM schemes at  $f_s= 2$  and 20 KHz

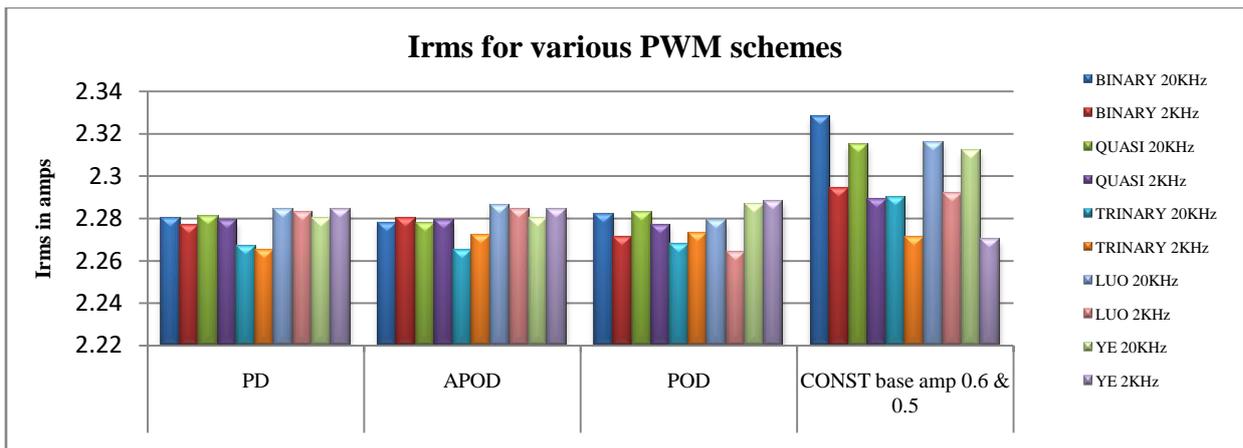


Fig 5.7 (a) RMS value of Irms for various PWM schemes for  $m_a = 1$  at  $f_s= 2$  and 20 KHz

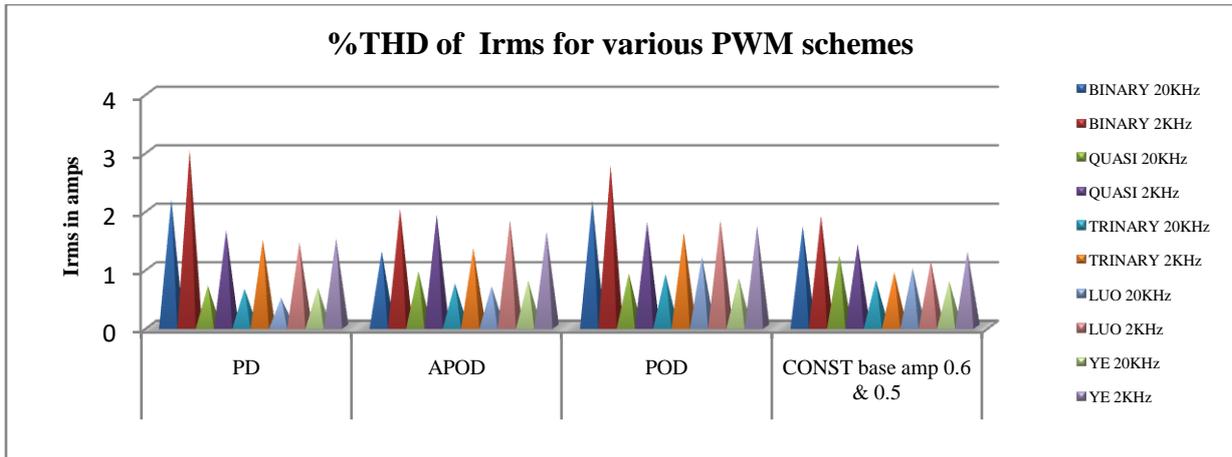


Fig 5.7 (b) %THD of Irms for various PWM schemes for  $m_a = 1$  at  $f_s= 2$  and 20 KHz

The above charts summarize the performances of the MLC for the switching frequency of 2 KHz and 20 KHz. The PD PWM technique shows reduced harmonics in currents than other techniques. The CC technique shows reduced harmonics in line and phase voltages less than 5% compared to other progression schemes. As a whole CC technique proves to perform better for improving the amplitudes of voltage and current parameters and also reduction in % THD. Among the triangular carrier techniques PD performs well for harmonic reduction and POD technique for improving the amplitudes of output voltage and current parameters at 20 KHz than 2 KHz.

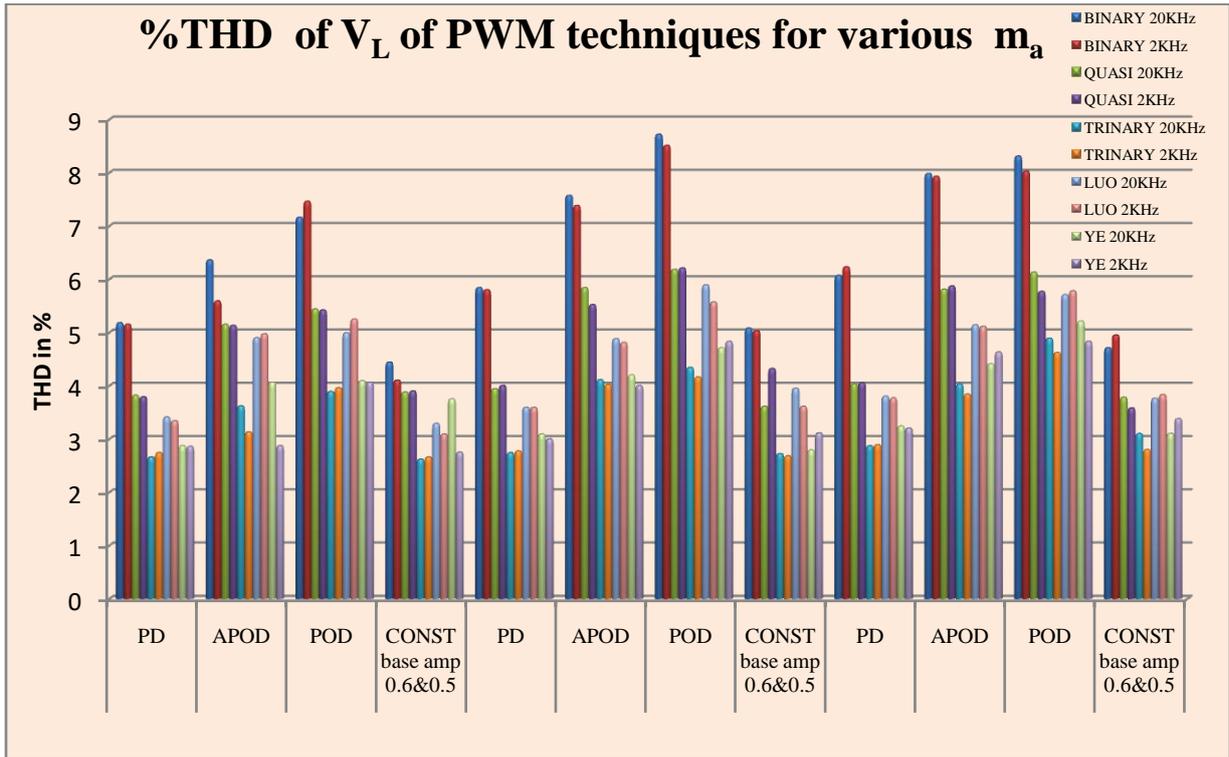


Fig 5.8 THD% of  $V_L$  of PWM techniques for various modulation index

The above fig 5.8 depicts that all the aforesaid PWM techniques gives better reduction in total harmonic distortion for the  $m_a = 1$  whereas when the  $m_a$  is less than 1, the % THD gets increased.

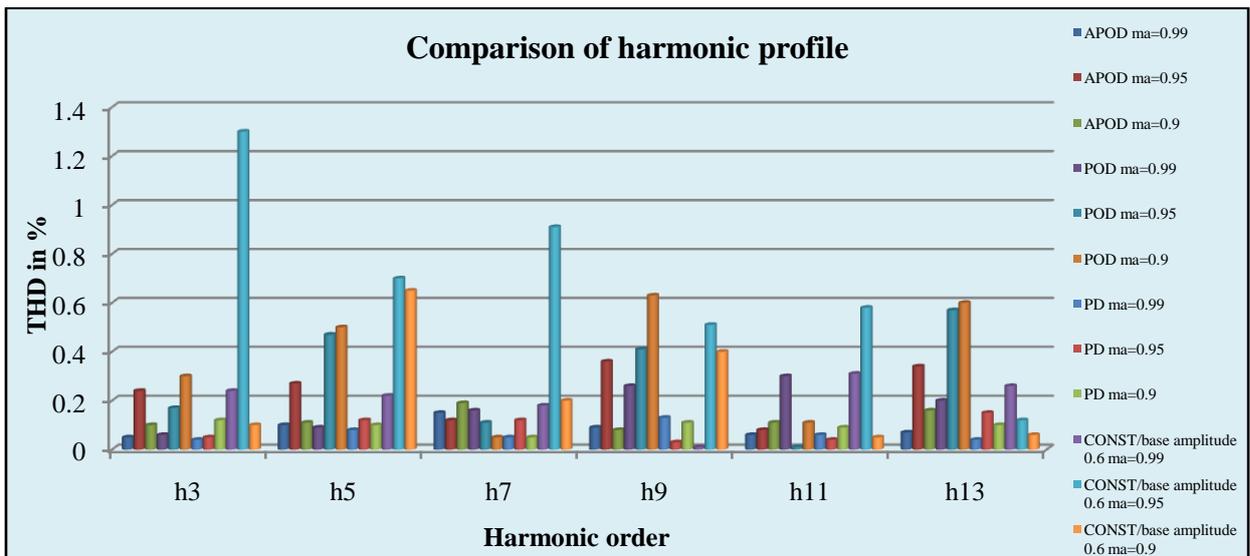


Fig 5.9 Comparison of harmonic profile of phase voltage obtained by YE progression for various PWM techniques at  $m_a = 1$  and  $f_{sw} = 20$  KHz

The fig 5.9 shown above depicts the occurrence of lower order harmonics in the output voltage. It is noted that though the CC technique has better reduction of %THD, the presence of lower order harmonics would be more for the modulation index less than one compared to other triangular carrier PWM techniques.

5.2 Comparisons based on overall performance of progression

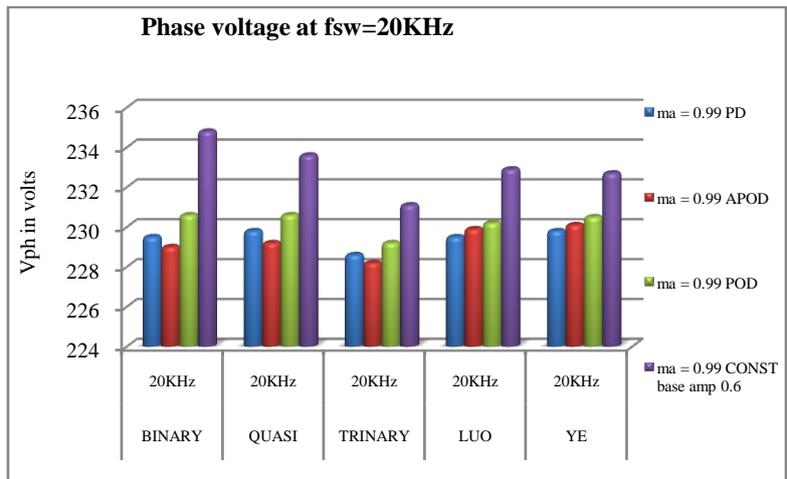


Fig 5.10 (a) Vph at fs=20 KHz

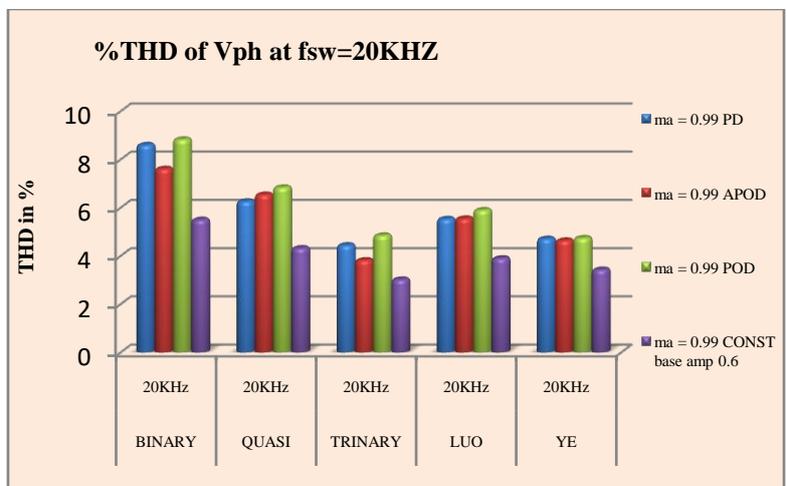


Fig 5.10 (b) %THD of Vph at fs =20 KHz

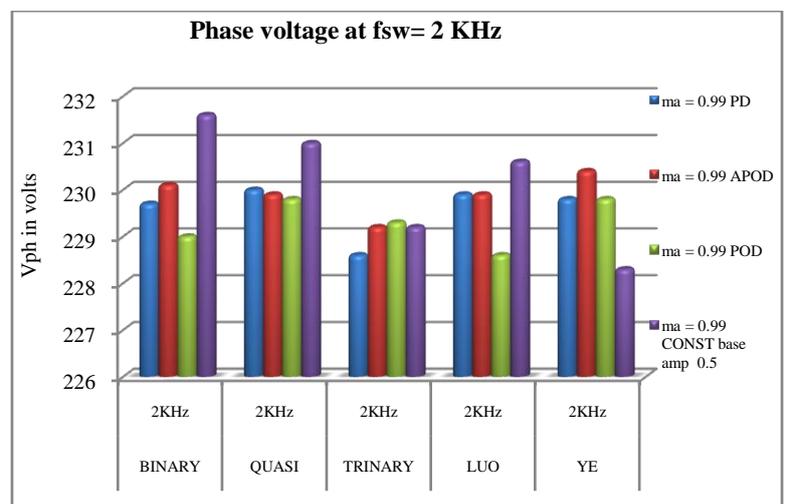


Fig 5.11 (a) Vph at fs= 2 KHz

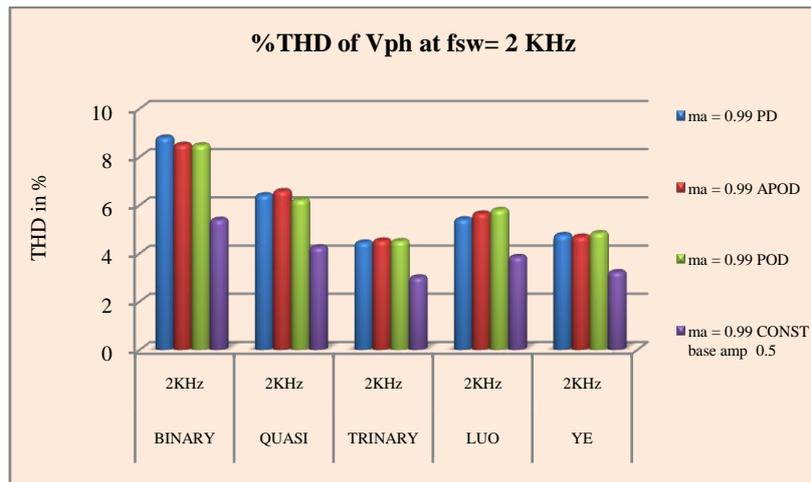


Fig 5.11 (b) %THD of Vph at fs= 2 KHz

All the above charts confer ranking for the PWM techniques and also for the progression schemes. Based on the generation of phase voltage binary or quasi, Ye, Luo and trinary has been ranked from high to low. But based on the reduction of harmonics the ranking may be given in the order of Trinary, Ye, Luo, quasi and binary.

## VI. Experimental Validation

A 3 $\phi$  cascaded 3 H Bridge system is implemented in real time using the real time interface controller dSPACE DS1103 to validate the performance of the aforesaid progression schemes. The DS1103 controller board is designed to meet the requirements of modern rapid control prototyping. The unparalleled number of I/O interfaces makes the DS1103 a versatile controller board for numerous applications. It provides a great selection of interfaces, including 50 bit-I/O channels, 36 A/D channels, and 8 D/A channels. It is possible to synchronize the A/D channels and D/A channels, with the I/O channels. In this experiment 32 digital I/O channels and 4 D/A channels are used to generate the switching pulses for the 36 switches (12 switches per phase).

The fig 6.1 shows the hardware setup of 3 $\phi$  cascaded 3 H Bridge system. Since complexity in using high dc sources, for this experimental setup the small dc power supply units have been selected based on trinary progression scheme as 2V, 6V, and 18V. Here the validation has been done with highest possible selection of voltage source progression is trinary progression.

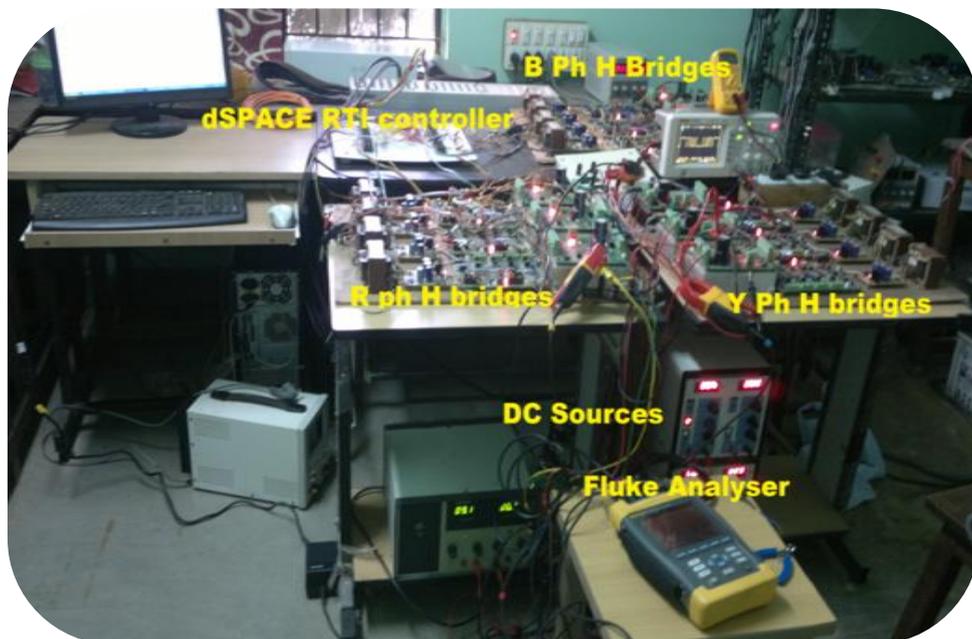


Fig 6.1 Experimental setup of 3 $\phi$  cascaded 3 H Bridge system

### 6.1 Experimental results using Fluke analyzer

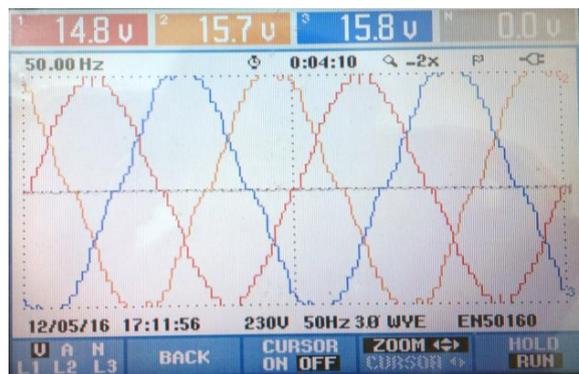
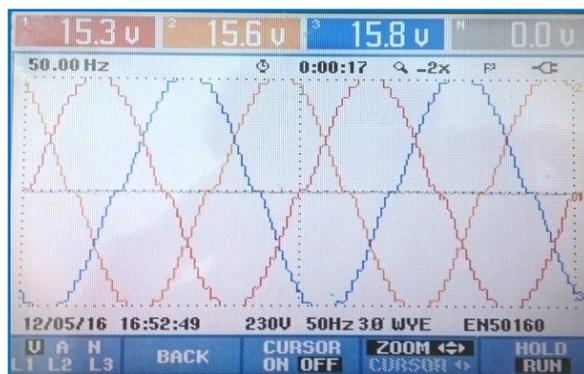


Fig 6.2 (a) Trinary Vph wave form by APOD at  $f_s=2$  KHz,  $m_a=1$



3Fig 6.3 (a) Trinary Vph wave form by POD at  $f_s=2$  KHz

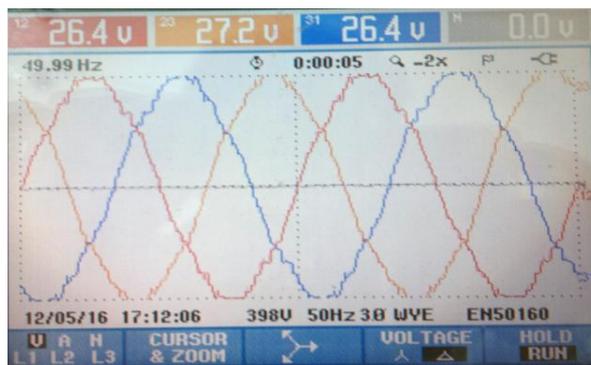


Fig 6.2 (b) 27 level Trinary line to line voltage waveform by APOD technique,  $f_s=2$  KHz,  $m_a=1$

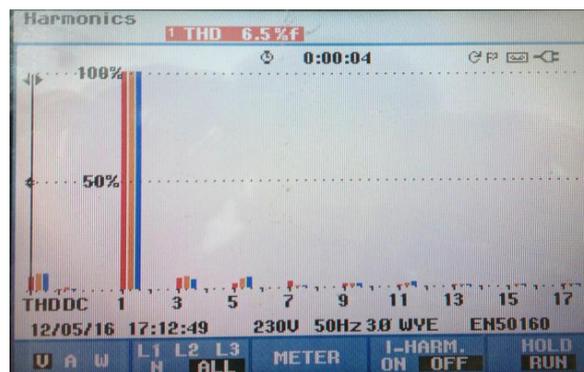


Fig 6.2 (c) Harmonic profile of Vph by APOD technique

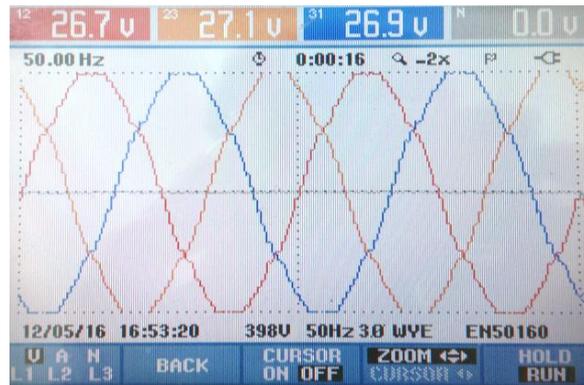


Fig 6.3 (b) 27 level Trinary line to line voltage waveform by POD technique,  $f_s=2$  KHz,  $m_a=1$



Fig 6.3 (c) Harmonic profile of  $V_{ph}$  by POD technique

The experimental results shown in fig 6.1 and fig 6.2 (a) to (c) depicts 27 level phase voltages, line to line voltage waveform and %THD of the output phase voltage obtained for trinary progression by APOD and POD technique respectively. The experimental results have been almost similar to simulation results. Thereby once again the trinary progression scheme has proven that it has produced the output with less harmonic content than other progression schemes.

## VII. Conclusion

This work has presented a number of asymmetrical topologies for multilevel inverters (MLI), some of them well known with applications on the market. Among all progression schemes the trinary scheme has generates higher levels in output and consequently the %THD in output voltage is very low when compared with other schemes. The arrangements of amplitude of voltage sources are different for similar system for each progression scheme. Hence the voltage stress on the switches is more for smaller level schemes. While all progressions work for a dissimilar system difference in amplitude of voltage source is high, as a result the rating of switches should be high for higher level schemes. By this analysis based on the overall performance the Trinary progression is much competent of producing fine AC output and followed by Ye, Luo, quasi and binary.

## Acknowledgement



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